AMENDMENT TO THE CLAIMS

1-5. (Canceled)

6. (Previously Presented) A method for fabricating a semiconductor device, comprising the steps of:

(a) epitaxially growing a p-type second single-crystal semiconductor layer functioning as a base layer on an n-type first single-crystal semiconductor layer functioning as a collector layer on a substrate;

(b) epitaxially growing a third single-crystal semiconductor layer on the second single-crystal semiconductor layer;

(c) depositing an emitter lead electrode by sequentially laminating an n^- polysilicon layer and an n^+ polysilicon layer, the n^- polysilicon layer containing phosphorus in a concentration equal to or lower than a concentration permitting phosphorus to be diffused into the third single-crystal semiconductor layer in a concentration as high as the solid-solubility limit for the third single-crystal semiconductor layer, and the n^+ polysilicon layer containing phosphorus in a concentration higher than that in the n^- polysilicon layer; and

(d) performing heat treatment for diffusing phosphorus in the n^- polysilicon layer so that the upper portion of the third single-crystal semiconductor layer is doped with phosphorus in a concentration equal to or lower than the solid-solubility limit, to form an emitter.

7. (Original) The method for fabricating a semiconductor device of claim 6, wherein in the step (c), the concentration of phosphorus introduced into the semiconductor layer is increased in stages toward the upper portion.

8. (Original) The method, for fabricating a semiconductor device of claim 6, wherein in the step (c), the concentration of phosphorus introduced into the semiconductor layer is increased sequentially toward the upper portion.

9. (Previously Presented) The method for fabricating a semiconductor device of claim 6, wherein

the first single-crystal semiconductor layer is a Si layer,

the second single-crystal semiconductor layer is a SiGe layer, and

the third single-crystal semiconductor layer is a Si layer.

10. (Previously Presented) The method for fabricating a semiconductor device of claim 6, wherein

the first single-crystal semiconductor layer is a Si layer,

the second single-crystal semiconductor layer is a SiGeC layer, and

the third single-crystal semiconductor layer is a Si layer.

11. (Cancelled)

12. (Currently Amended) ~~The method for fabricating a semiconductor device of claim 11,~~ A method for fabricating a semiconductor device comprising the steps of:

(a) epitaxially growing a p-type second single-crystal semiconductor layer functioning as a base layer on an n-type first single-crystal semiconductor layer functioning as a collector layer on a substrate;

(b) epitaxially growing a third single-crystal semiconductor layer on the second single-crystal semiconductor layer;

(c) doping at least an upper portion of the third single-crystal semiconductor layer with a p-type impurity;

(d) forming a semiconductor layer containing phosphorus on the third single-crystal semiconductor layer; and

(e) performing heat treatment for diffusing phosphorus in the semiconductor layer so that the upper portion of the third single-crystal semiconductor layer is doped with phosphorus in a concentration higher than the concentration of the p-type impurity introduced in the step (c), to change the upper portion of the third single-crystal semiconductor layer into an emitter,

wherein the step (c) is performed simultaneously with the step (b) by epitaxially growing the third single-crystal semiconductor layer while being doped with the p-type impurity.

13. (Cancelled)

14. (Currently Amended) [[The]] A method for fabricating a semiconductor device ~~of claim 11, further~~ comprising the steps of:

(a) epitaxially growing a p-type second single-crystal semiconductor layer functioning as a base layer on an n-type first single-crystal semiconductor layer functioning as a collector layer on a substrate;

(b) epitaxially growing a third single-crystal semiconductor layer on the second single-crystal semiconductor layer;

(c) doping at least an upper portion of the third single-crystal semiconductor layer with a p-type impurity;

(d) forming a semiconductor layer containing phosphorus on the third single-crystal semiconductor layer;

(e) performing heat treatment for diffusing phosphorus in the semiconductor layer so that the upper portion of the third single-crystal semiconductor layer is doped with phosphorus in a concentration higher than the concentration of the p-type impurity introduced in the step (c), to change the upper portion of the third single-crystal semiconductor layer into an emitter;

(f) forming an insulating layer on the third single-crystal semiconductor layer after the step (b) and before the step (c); and

(g) forming a semiconductor layer containing a p-type impurity on the insulating layer,

wherein the step (c) is performed by introducing the p-type impurity into the third single-crystal semiconductor layer from the semiconductor layer via the insulating layer.

15. (Previously Presented) The method for fabricating a semiconductor device of claim 6, wherein the n^- polysilicon layer has a recessed part and the n^+ polysilicon layer has a protruded part, and

the emitter lead electrode is deposited to fit the recessed part to the protruded part.